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## 150mA 2ch LDO REGULATOR

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NO.EA-089-0607

### OUTLINE

The R5323x Series are CMOS-based voltage regulator ICs with high output voltage accuracy, low supply current, low dropout, and high ripple rejection. Each of these voltage regulator ICs consists of a voltage reference unit, an error amplifier, resistors for setting Output Voltage, a current limit circuit, and a chip enable circuit.

These ICs perform with low dropout voltage due to built-in transistor with low ON resistance, and a chip enable function prolongs the battery life of each system. The line transient response and load transient response of the R5323x Series are excellent, thus these ICs are very suitable for the power supply for hand-held communication equipment.

The output voltage of these ICs is internally fixed with high accuracy. Since the packages for these ICs are SOT-23-6, PLP1820-6 and WL-CSP-6 package, 2ch LDO regulators are included in each package, high density mounting of the ICs on boards is possible.

### FEATURES

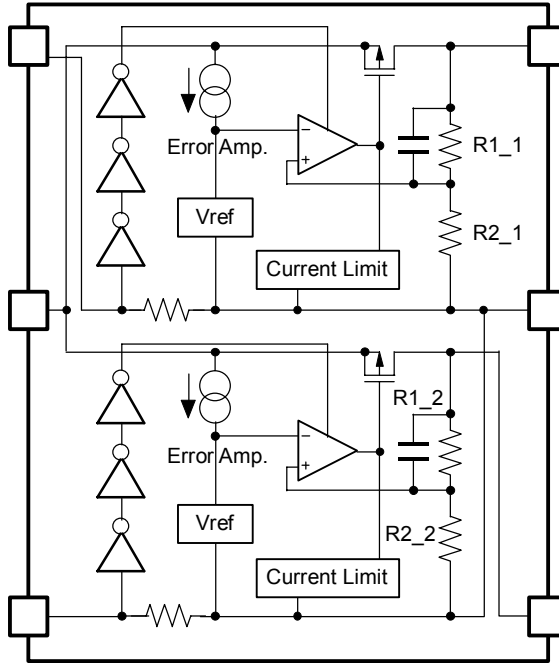
- Low Supply Current ..... Typ. 90 $\mu$ A (VR1, VR2)
- Standby Mode ..... Typ. 0.1 $\mu$ A (VR1, VR2)
- Low Dropout Voltage ..... Typ. 0.22V ( $I_{OUT}=150\text{mA}$ , Output Voltage Type)
- High Ripple Rejection ..... Typ. 75dB( $V_{OUT} \leq 2.4\text{V}$ ), Typ. 70dB( $V_{OUT} \leq 2.5\text{V}$ ) ( $f=1\text{kHz}$ )  
Typ. 65dB( $V_{OUT} \leq 2.4\text{V}$ ), Typ. 60dB( $V_{OUT} \leq 2.5\text{V}$ ) ( $f=10\text{kHz}$ )
- Low Temperature-drift Coefficient of Output Voltage .... Typ.  $\pm 100\text{ppm}/^\circ\text{C}$
- Excellent Line Regulation ..... Typ. 0.02%/V
- High Output Voltage Accuracy .....  $\pm 2.0\%$
- Small Packages ..... SOT-23-6, PLP1820-6, WL-CSP-6
- Output Voltage ..... Stepwise setting with a step of 0.1V in the range of 1.5V to 4.0V is possible
- Built-in chip enable circuit (A/B: active high)
- Built-in fold-back protection circuit ..... Typ. 40mA (Current at short mode)
- Ceramic Capacitor is recommended. (1.0 $\mu$ F or more)

### APPLICATIONS

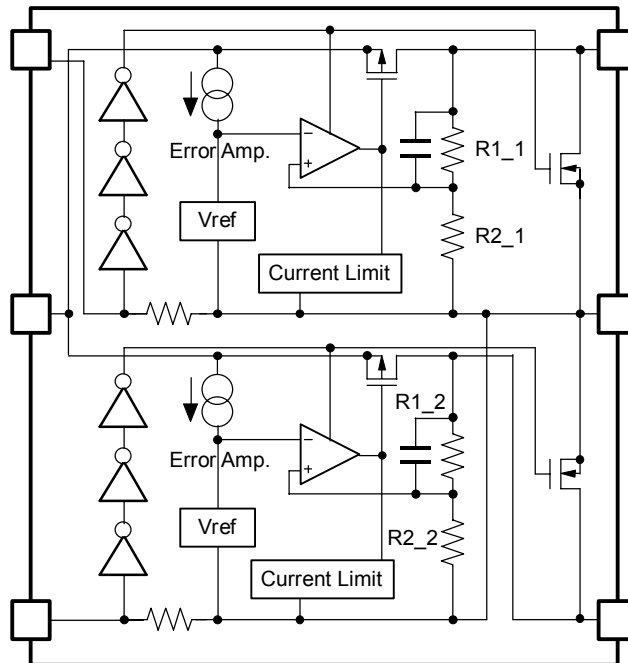
- Power source for handheld communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for battery-powered equipment.

BLOCK DIAGRAMS

R5323xxxxA



R5323xxxxB



## SELECTION GUIDE

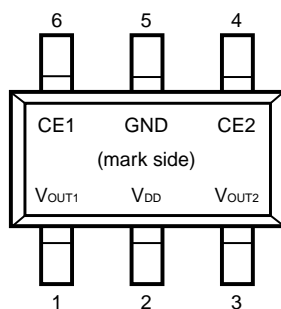
The output voltage, mask option, and the taping type for the ICs can be selected at the user's request. The selection can be made with designating the part number as shown below;

R5323xxxxx-xx-X ←Part Number  
 ↑ ↑ ↑ ↑ ↑  
 a b c d e

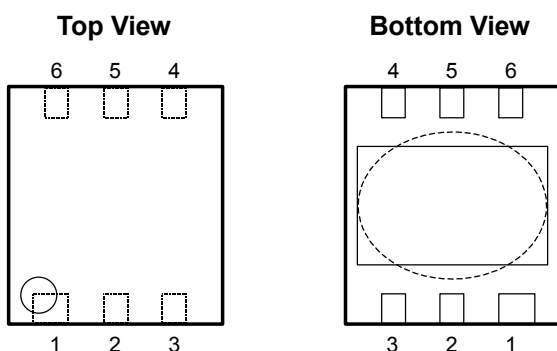
Code	Contents
a	Designation of Package Type: N : SOT-23-6 K : PLP1820-6 Z : WL-CSP-6
b	Setting combination of 2ch Output Voltage ( $V_{OUT}$ ) : Serial Number for Voltage Setting, Stepwise setting with a step of 0.1V in the range of 1.5V to 4.0V is possible for each channel.
c	Designation of Mask Option: A version: without auto discharge function at OFF state. B version: with auto discharge function at OFF state.
d	Designation of Taping Type: Ex. TR (refer to Taping Specifications; TR type is the standard direction.)
e	Designation of composition of plating: -F : Lead free plating (SOT-23-5,WL-CSP-6) None : Au plating (PLP1820-6)

## PIN CONFIGURATION

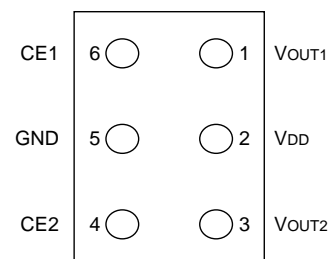
### ● SOT-23-6



### ● PLP1820-6



### ● WLCSP-6




## PIN DESCRIPTIONS

### • SOT-23-6

Pin No.	Symbol	Description
1	V <sub>OUT1</sub>	Output Pin 1
2	V <sub>DD</sub>	Input Pin
3	V <sub>OUT2</sub>	Output Pin 2
4	CE2	Chip Enable Pin 2
5	GND	Ground Pin
6	CE1	Chip Enable Pin 1

### PLP1820-6

Pin No.	Symbol	Description
1	V <sub>OUT2</sub>	Output Pin 2
2	V <sub>DD</sub>	Input Pin
3	V <sub>OUT1</sub>	Output Pin 1
4	GND	Ground Pin
5	CE1	Chip Enable Pin 1
6	CE2	Chip Enable Pin 2

\* Tab in the:  parts have GND level.  
(They are connected to the reverse side of this IC.)  
Do not connect to other wires or land patterns.

### • WLCSP-6

Pin No.	Symbol	Description
1	V <sub>OUT1</sub>	Output Pin 1
2	V <sub>DD</sub>	Input Pin
3	V <sub>OUT2</sub>	Output Pin 2
4	CE2	Chip Enable Pin 2
5	GND	Ground Pin
6	CE1	Chip Enable Pin 1

## ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V <sub>IN</sub>	Input Voltage	6.5	V
V <sub>CE</sub>	Input Voltage (CE Pin)	6.5	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>IN</sub> + 0.3	V
I <sub>OUT1</sub>	Output Current 1	200	mA
I <sub>OUT2</sub>	Output Current 2	200	mA
P <sub>D</sub>	Power Dissipation (SOT-23-6)*1	420	mW
	Power Dissipation (PLP1820-6) *1	880	
	Power Dissipation (WL-CSP-6)	633	
T <sub>opt</sub>	Operating Temperature Range	-40 to 85	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to 125	°C

\*1 For Power Dissipation, please refer to PACKAGE INFORMATION to be described.

## ELECTRICAL CHARACTERISTICS

### • R5323xxxxA/B

T<sub>opt</sub>=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>OUT</sub>	Output voltage	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V 1mA ≤ I <sub>OUT</sub> ≤ 30mA	V <sub>OUT</sub> ×0.98		V <sub>OUT</sub> ×1.02	V
I <sub>OUT</sub>	Output Current	V <sub>IN</sub> -V <sub>OUT</sub> = 1.0V	150			mA
ΔV <sub>OUT</sub> /ΔI <sub>OUT</sub>	Load regulation	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V 1mA ≤ I <sub>OUT</sub> ≤ 150mA		15	40	mV
V <sub>DIF</sub>	Dropout Voltage	Refer to the Electrical Characteristics by Output Voltage				
I <sub>SS</sub>	Supply Current	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V		90	120	μA
I <sub>standby</sub>	Supply Current(Standby)	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V V <sub>CE</sub> =GND		0.1	1.0	μA
ΔV <sub>OUT</sub> /ΔV <sub>IN</sub>	Line regulation	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 6.0V I <sub>OUT</sub> =30mA		0.02	0.10	%/V
RR	Ripple Rejection	Ripple 0.5Vp-p V <sub>IN</sub> =Set V <sub>OUT</sub> +1V I <sub>OUT</sub> =30mA (In case that V <sub>OUT</sub> ≤ 1.7V, V <sub>IN</sub> =Set V <sub>OUT</sub> +1.2V)		75 *Note1  65 *Note2		dB
V <sub>IN</sub>	Input Voltage		2.0		6.0	V
ΔV <sub>OUT</sub> / ΔT <sub>opt</sub>	Output Voltage Temperature Coefficient	I <sub>OUT</sub> =30mA -40°C ≤ T <sub>opt</sub> ≤ 85°C		±100		ppm /°C
I <sub>lim</sub>	Short Current Limit	V <sub>OUT</sub> =0V		40		mA
R <sub>PD</sub>	Pull-down resistance for CE pin		0.7	2.0	8.0	MΩ
V <sub>CEH</sub>	CE Input Voltage "H"		1.5		6.0	V
V <sub>CEL</sub>	CE Input Voltage "L"		0.0		0.3	V
en	Output Noise	BW=10Hz to 100kHz		30		μVrms
R <sub>LOW</sub>	Low Output Nch Tr. ON Resistance (of B version)	V <sub>CE</sub> =0V		60		Ω

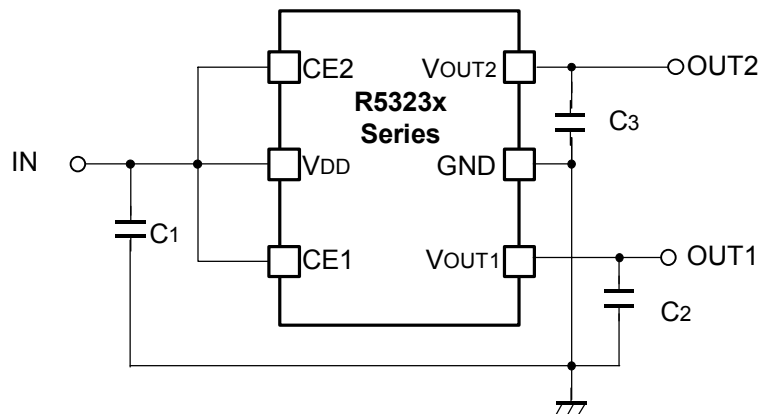
\*Note1: f=1kHz, 70dB as to V<sub>OUT</sub> ≥ 2.5V Output type.

\*Note2: f=10kHz, 60dB as to V<sub>OUT</sub> ≥ 2.5V Output type.

• Electrical Characteristics by Output Voltage

Output Voltage $V_{OUT}$ (V)	Dropout Voltage $V_{DIF}$ (V)		
	Condition	Typ.	Max.
$V_{OUT}=1.5$	$I_{OUT}=150mA$	0.38	0.70
$V_{OUT}=1.6$		0.35	0.65
$V_{OUT}=1.7$		0.33	0.60
$1.8V \leq V_{OUT} \leq 2.0V$		0.32	0.55
$2.1V \leq V_{OUT} \leq 2.7V$		0.28	0.50
$2.8V \leq V_{OUT} \leq 4.0V$		0.22	0.35

TYPICAL APPLIATION



(External Components)

Ceramic Capacitor Type  $C_1, C_2, C_3$

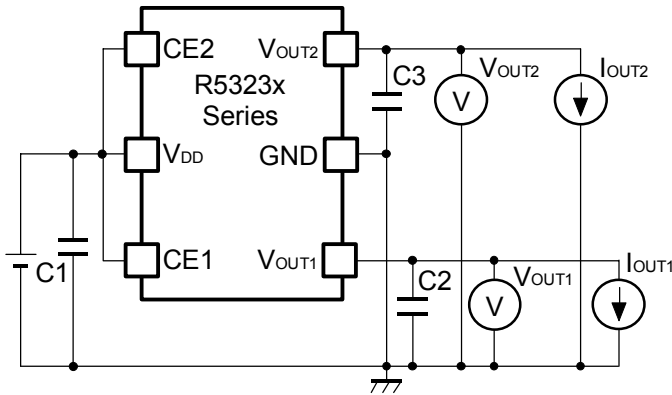
Recommended Ceramic capacitor for Output: GRM219R61A105K (Murata)

General Example of External Components

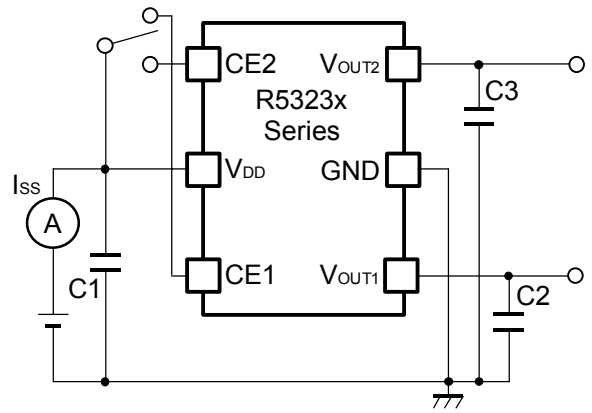
Ceramic Capacitors: C1608X5R0J105K (TDK)

GRM188R60J105K (Murata)

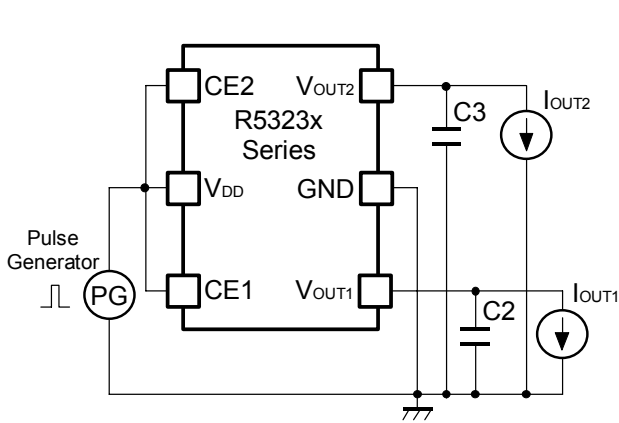
**TEST CIRCUIT**



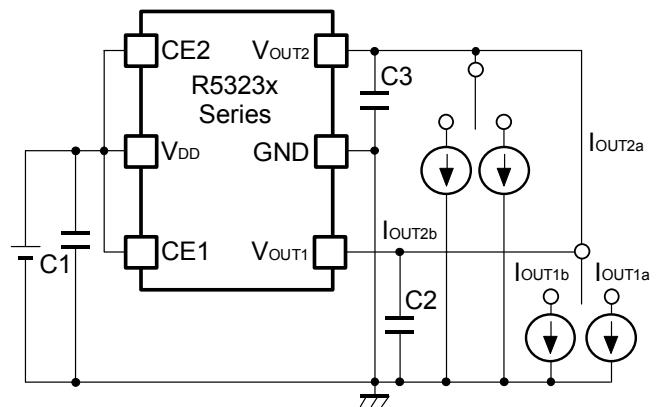
**Fig.1 Standard test Circuit**



**Fig.2 Supply Current Test Circuit**



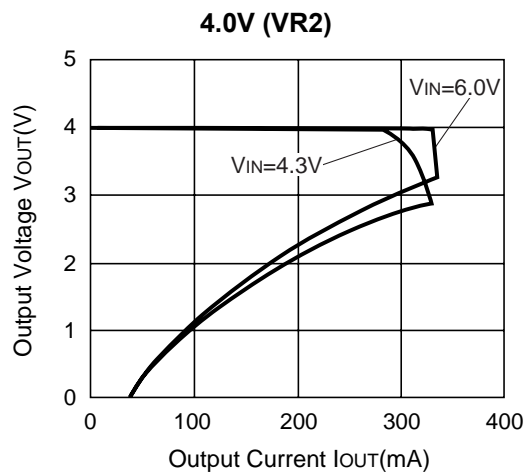
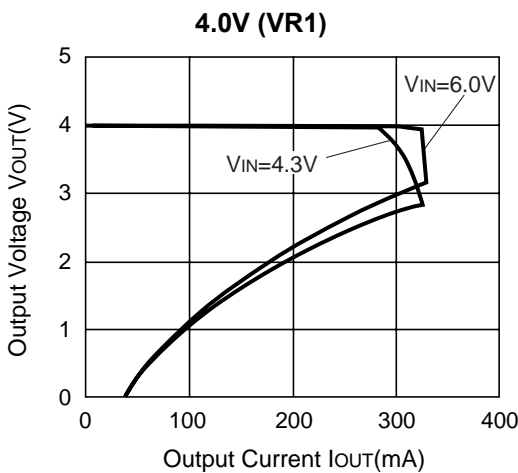
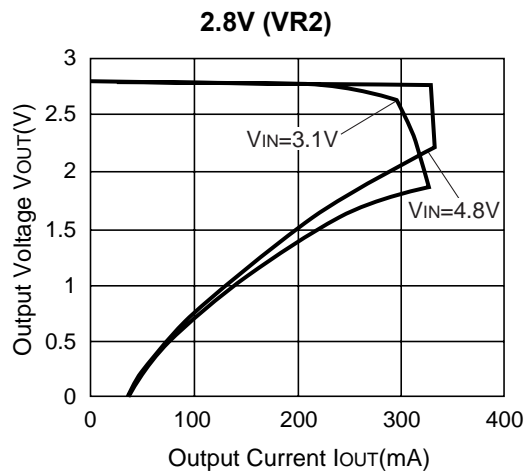
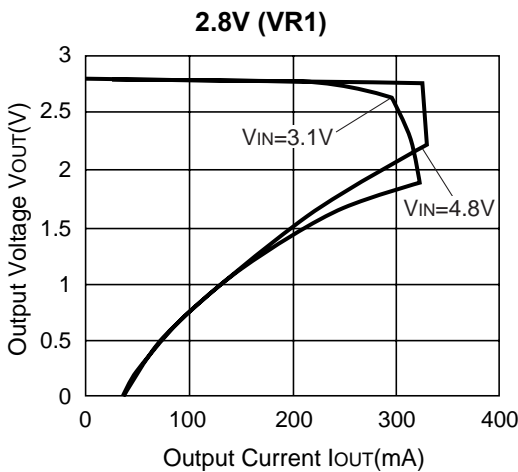
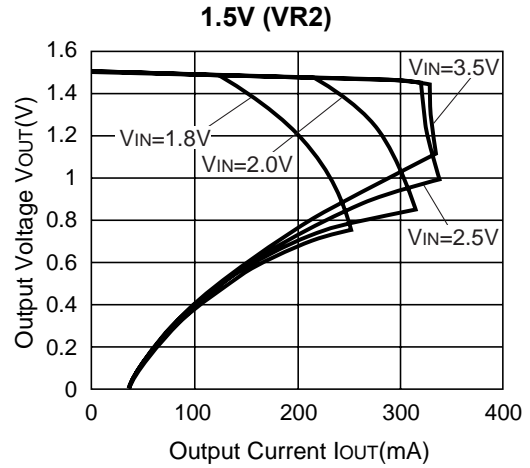
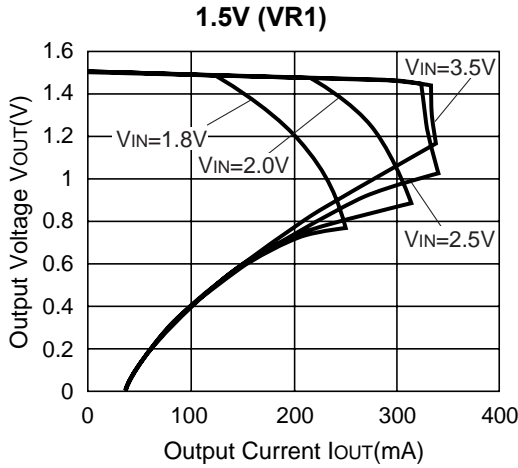
**Fig.3 Ripple Rejection, Line Transient Response Test Circuit**



**Fig.4 Load Transient Response Test Circuit**

## TYPICAL CHARACTERISTICS

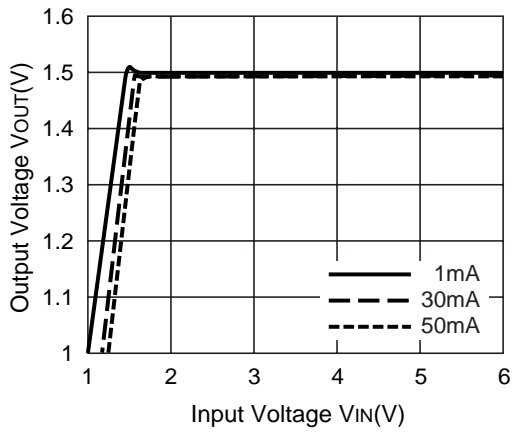
### 1) Output Voltage vs. Output Current (Topt=25°C)



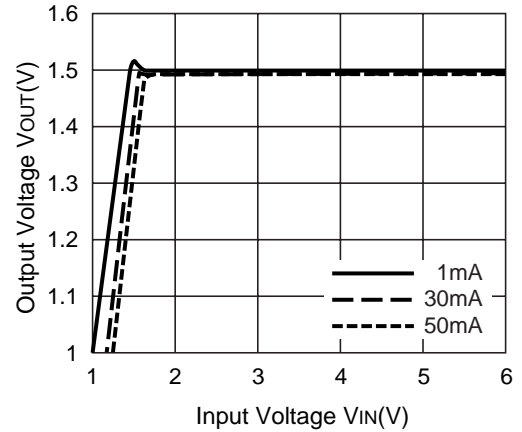


2) Output Voltage vs. Input Voltage (Topt=25°C)

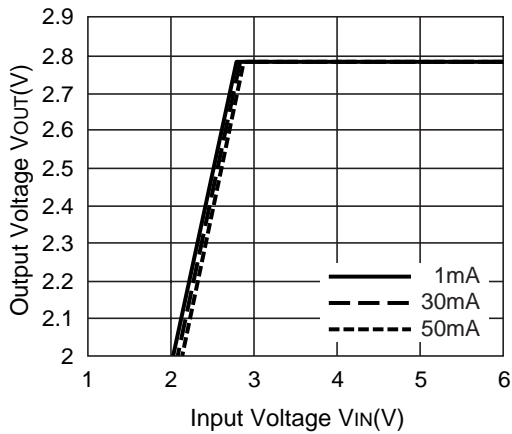
1.5V (VR1)



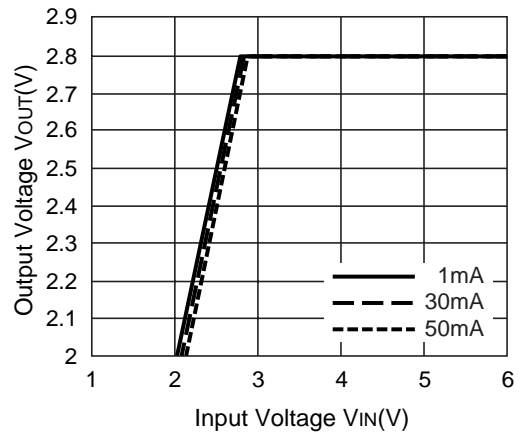
1.5V (VR2)



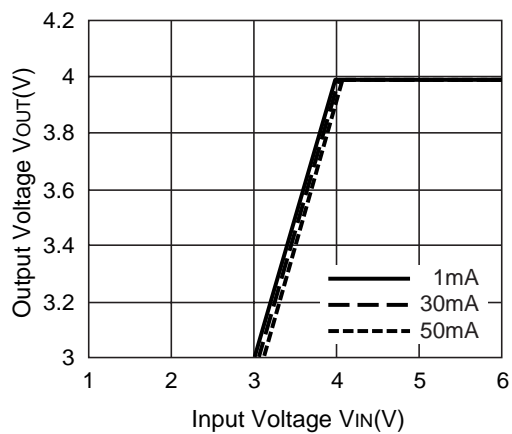
2.8V (VR1)



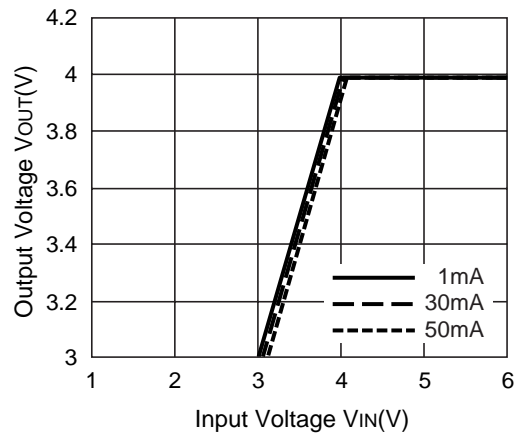
2.8V (VR2)



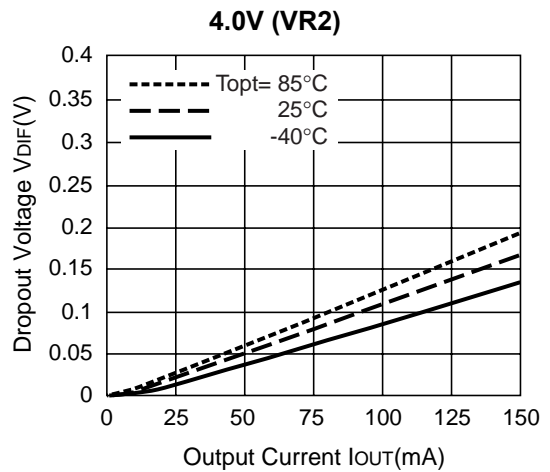
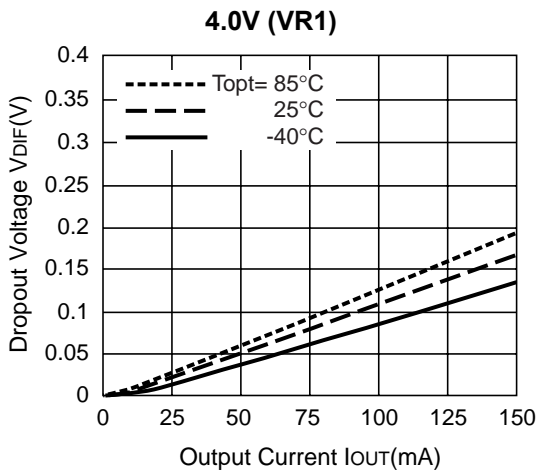
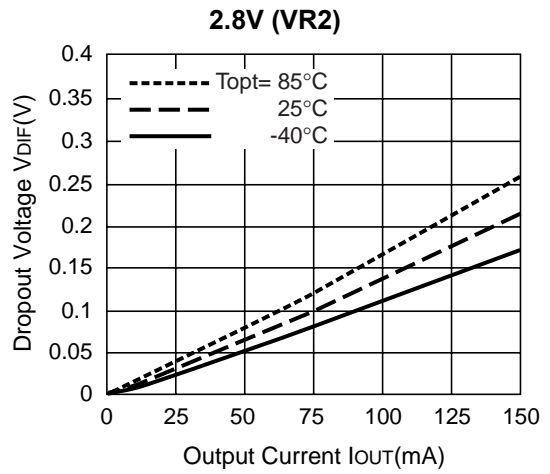
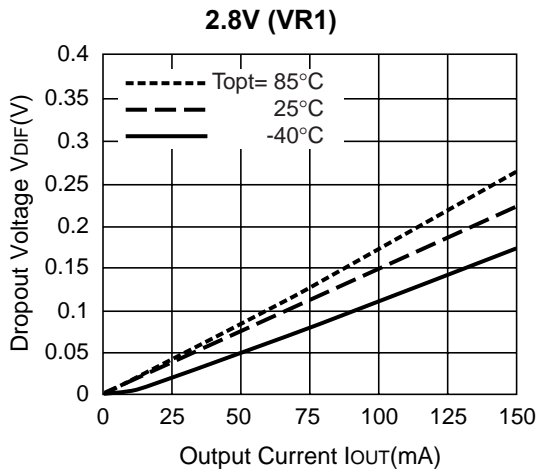
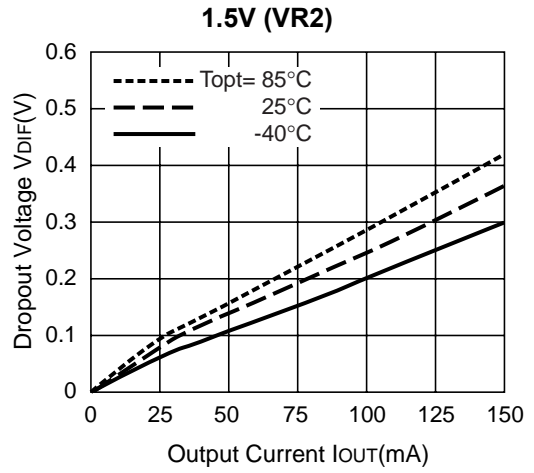
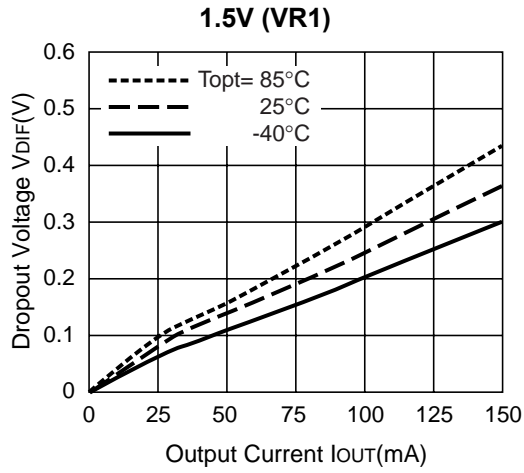
4.0V (VR1)



4.0V (VR2)

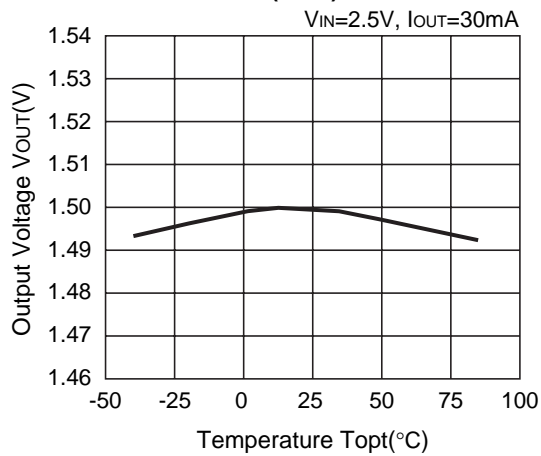


3) Dropout Voltage vs. Temperature

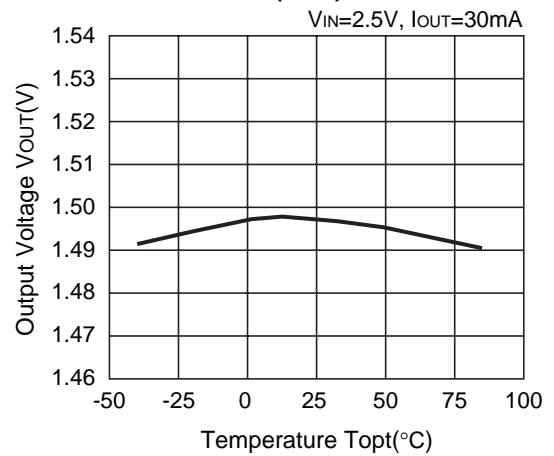


## 4) Output Voltage vs. Temperature

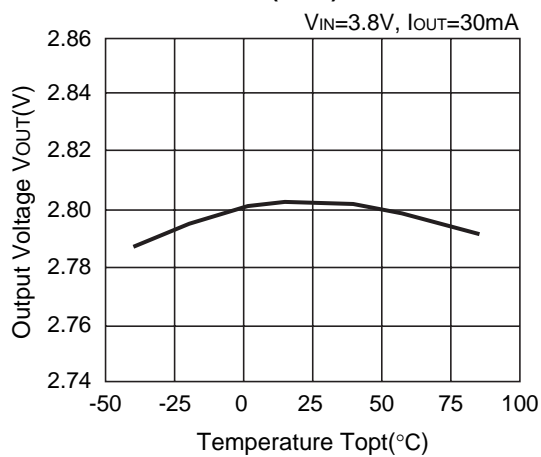
1.5V (VR1)



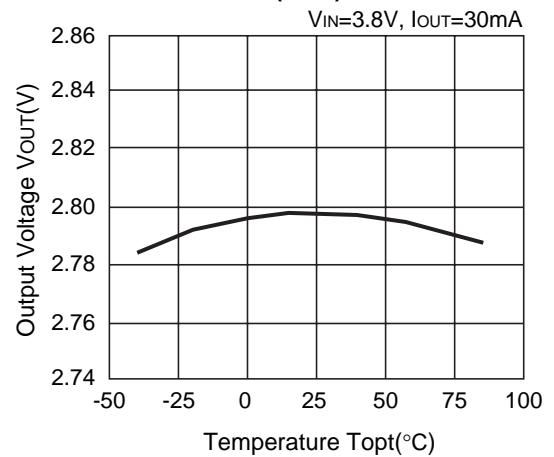
1.5V (VR2)



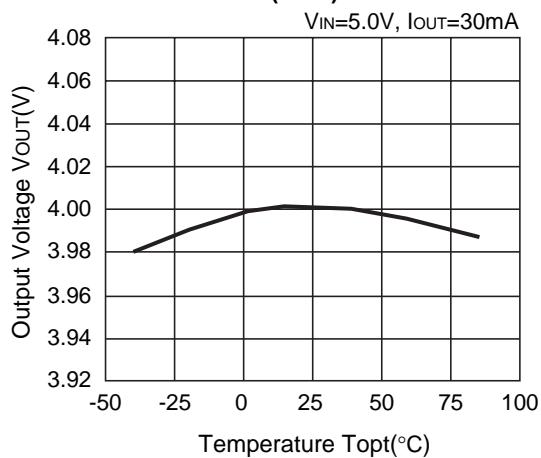
2.8V (VR1)



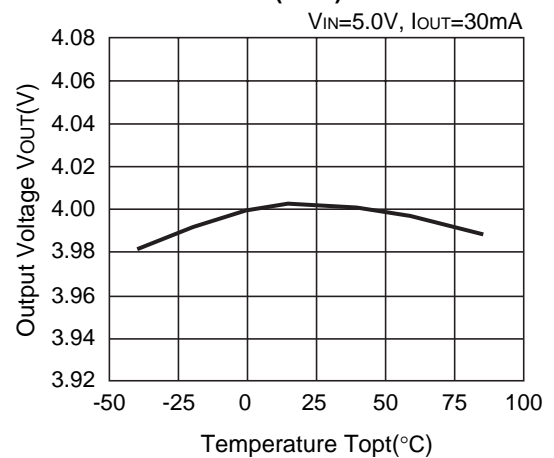
2.8V (VR2)



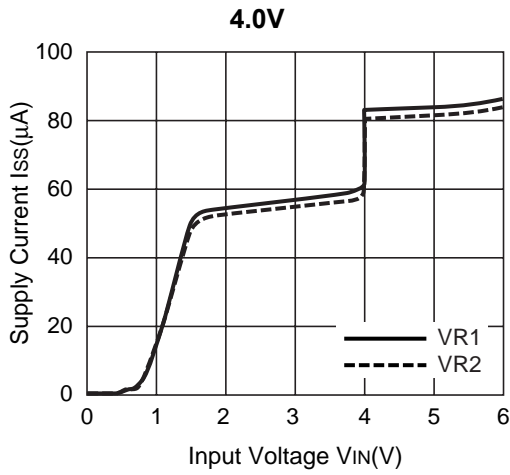
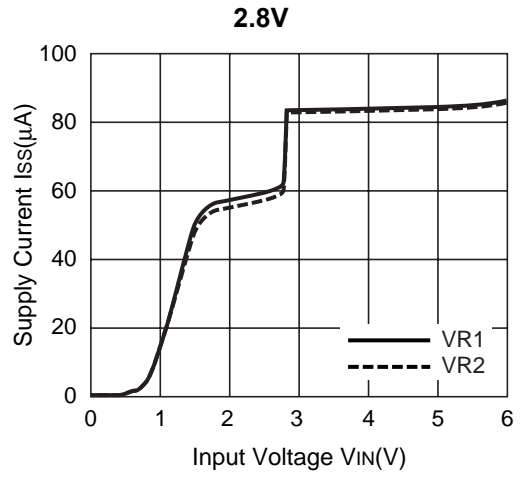
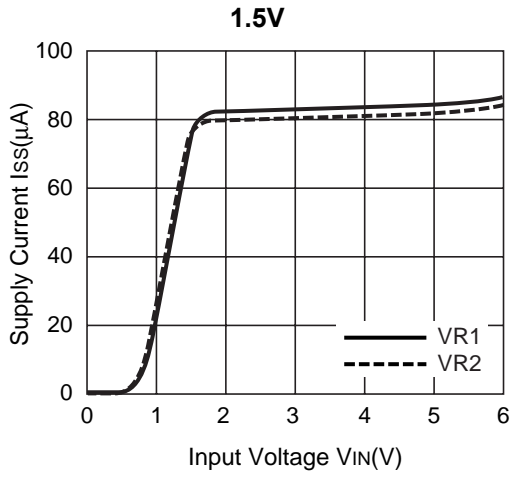
4.0V (VR1)



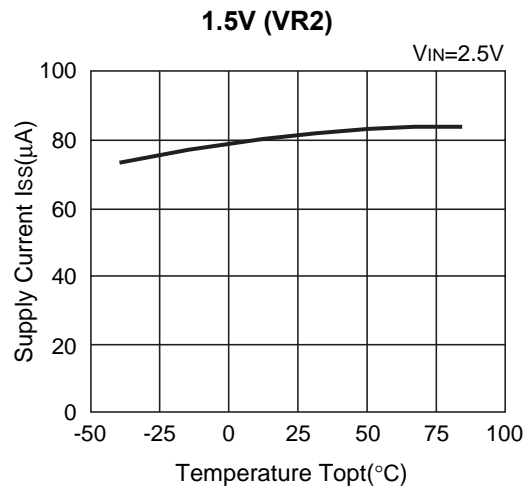
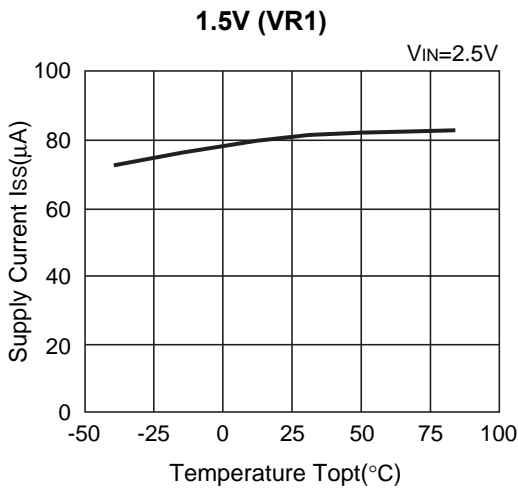
4.0V (VR2)

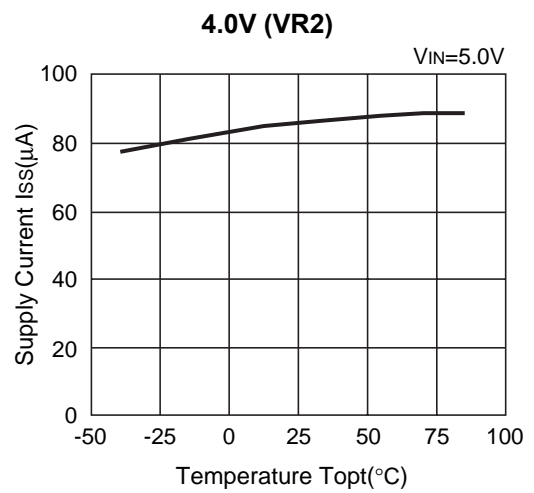
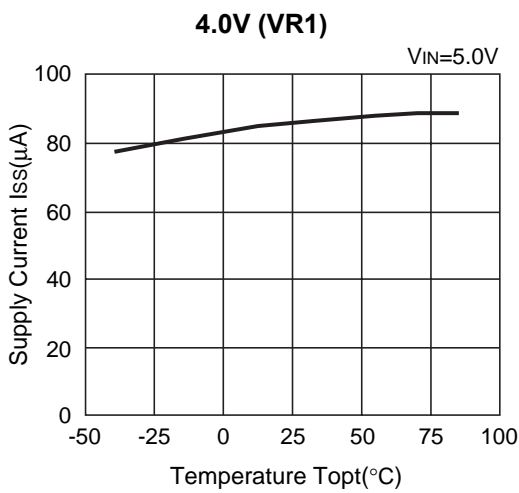
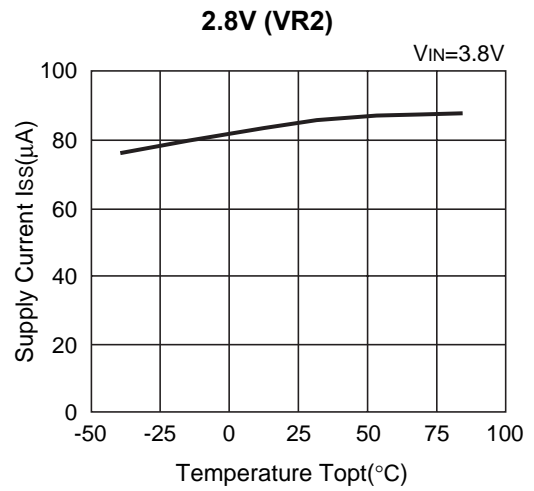
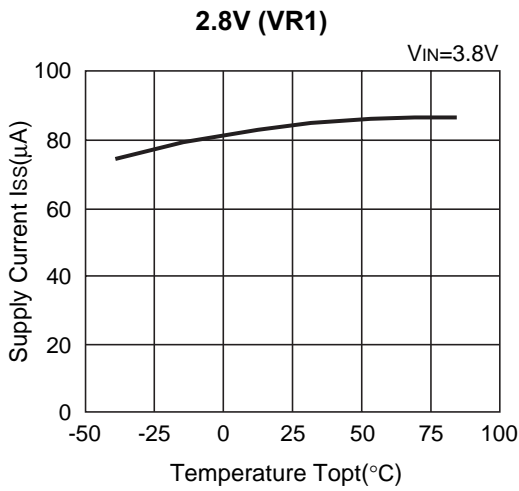


5) Supply Current vs. Input Voltage (Topt=25°C)

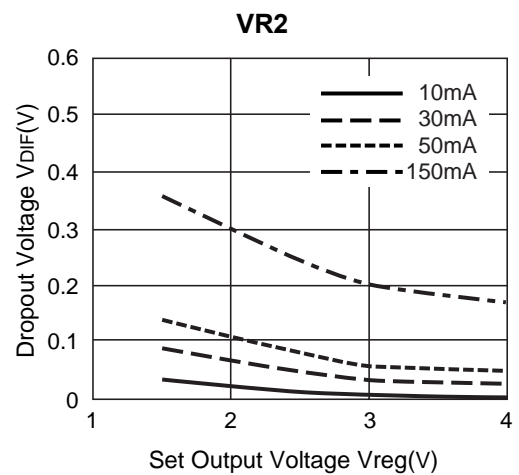
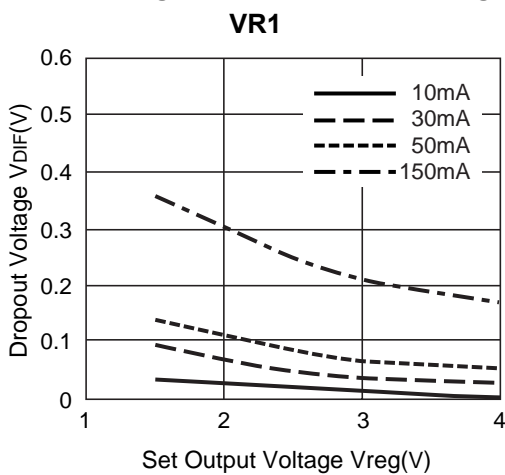


6) Supply Current vs. Temperature

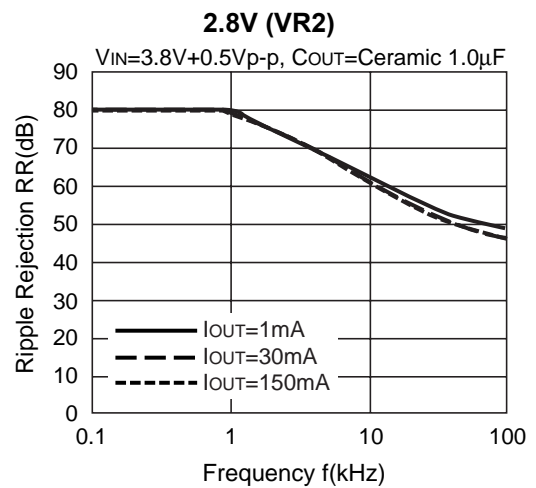
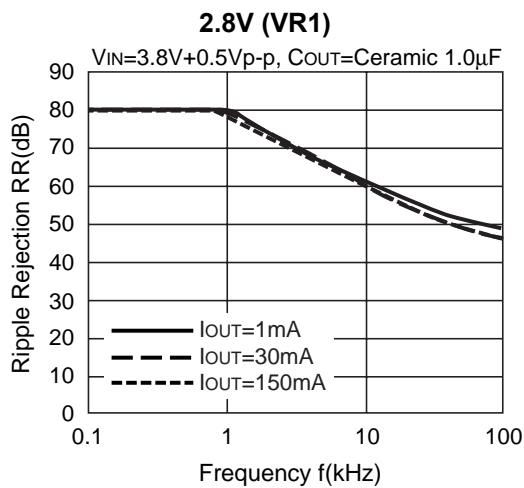
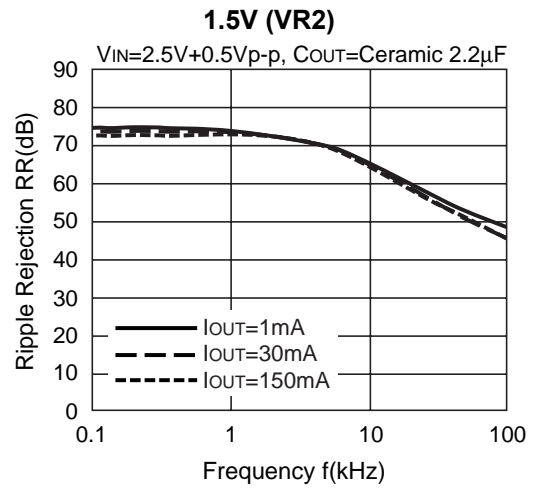
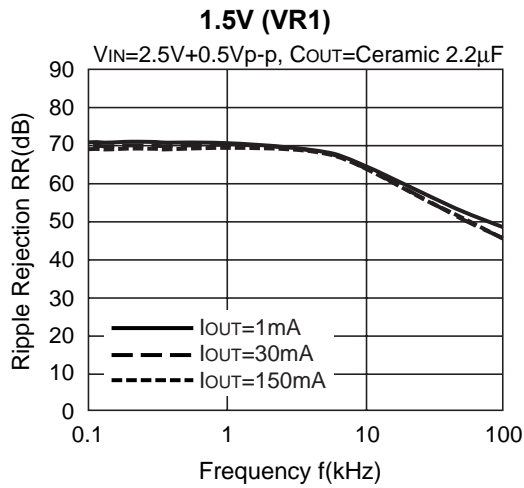
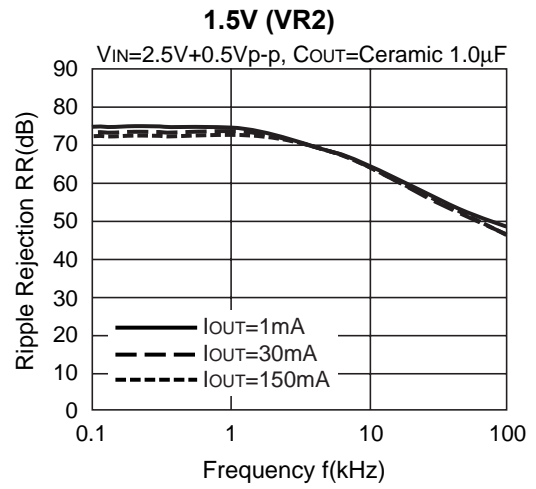
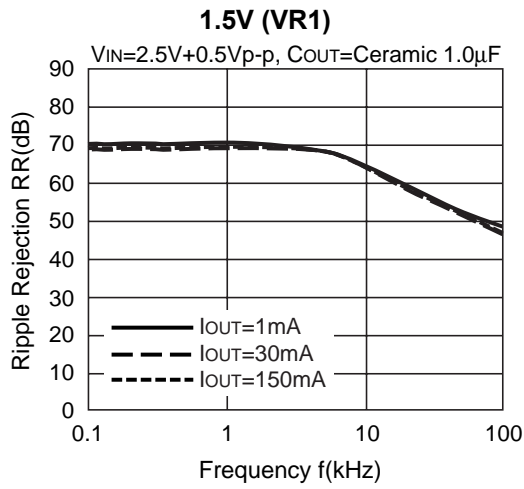


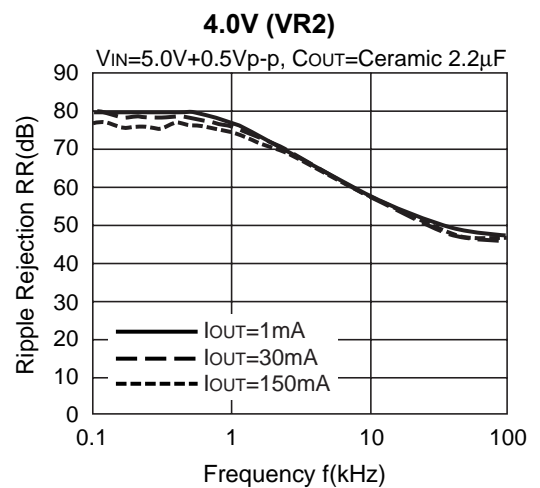
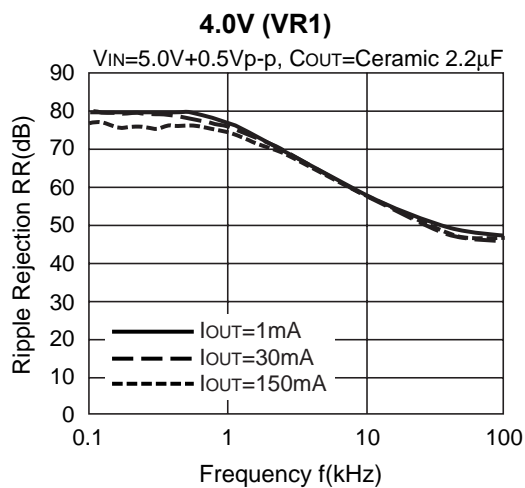
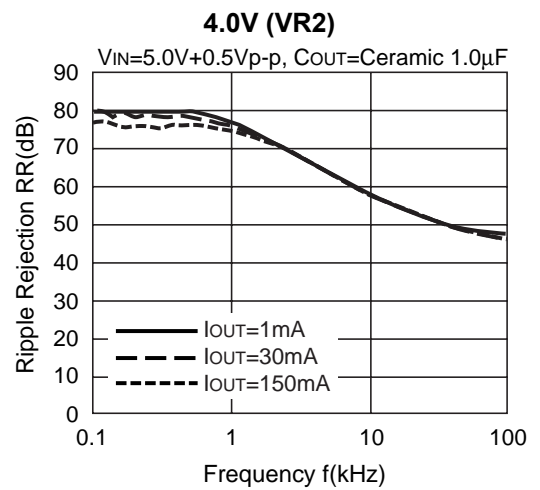
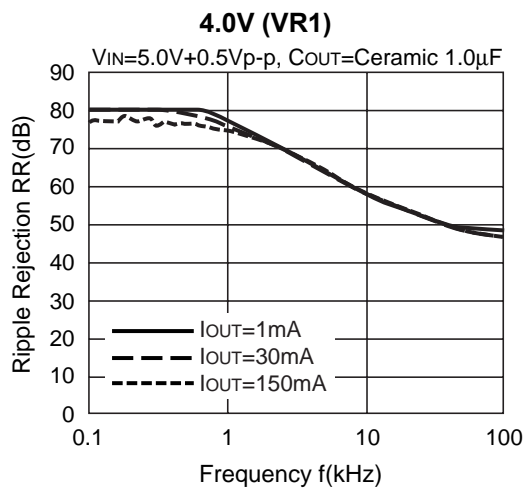
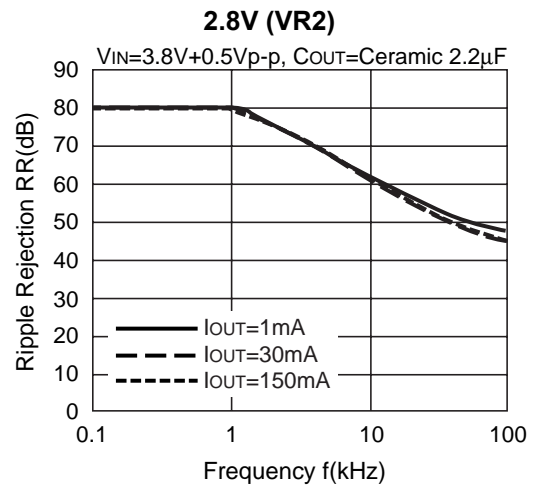
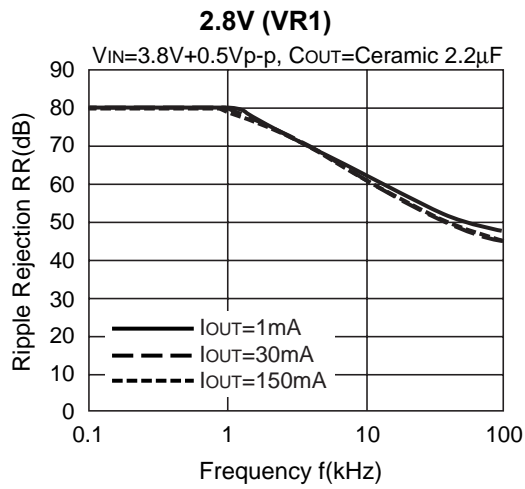


**7) Dropout Voltage vs. Set Output Voltage (T<sub>opt</sub>=25°C)**

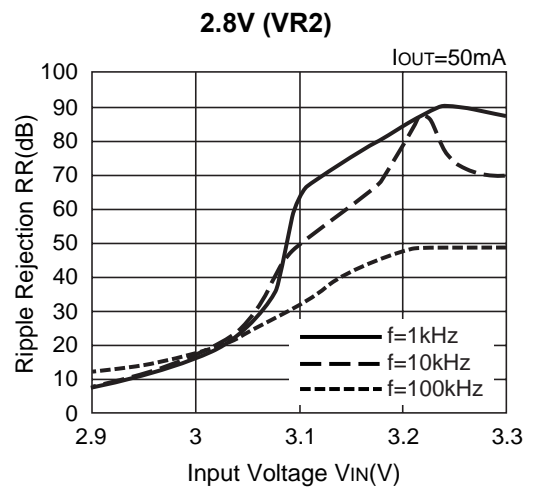
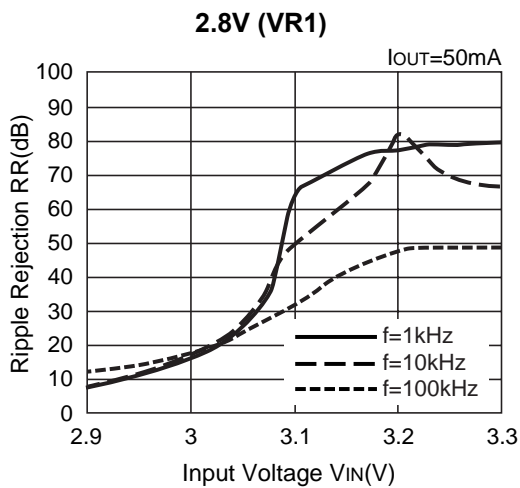
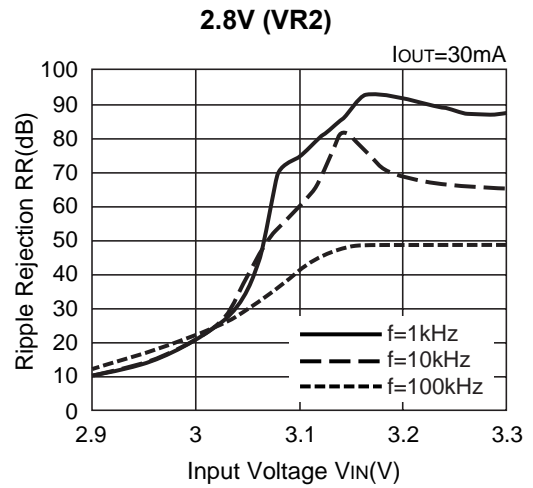
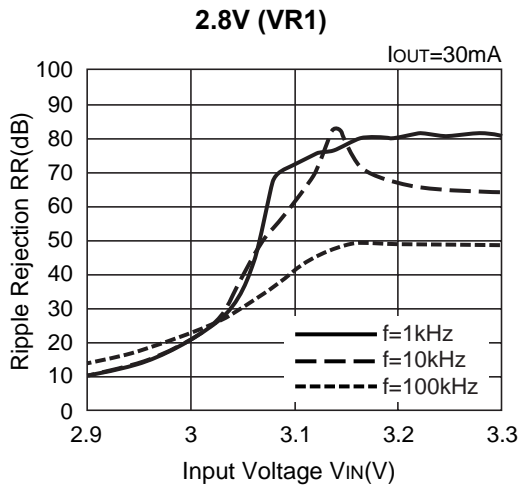
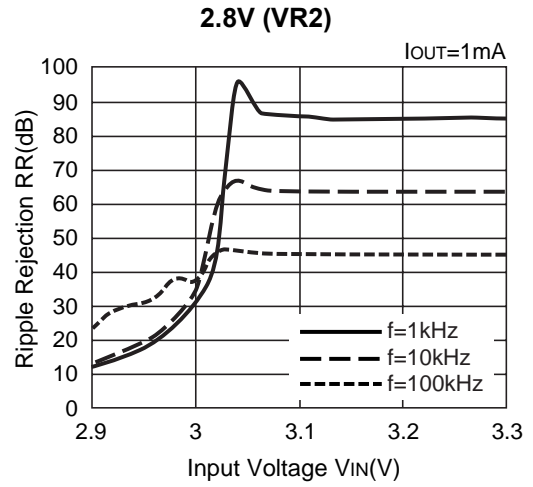
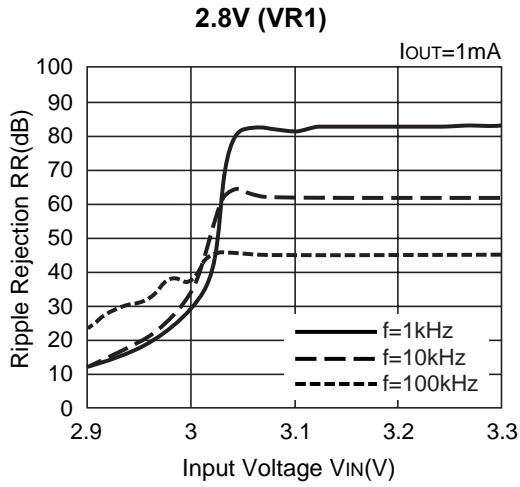


8) Ripple Rejection vs. Frequency (Topt=25°C)





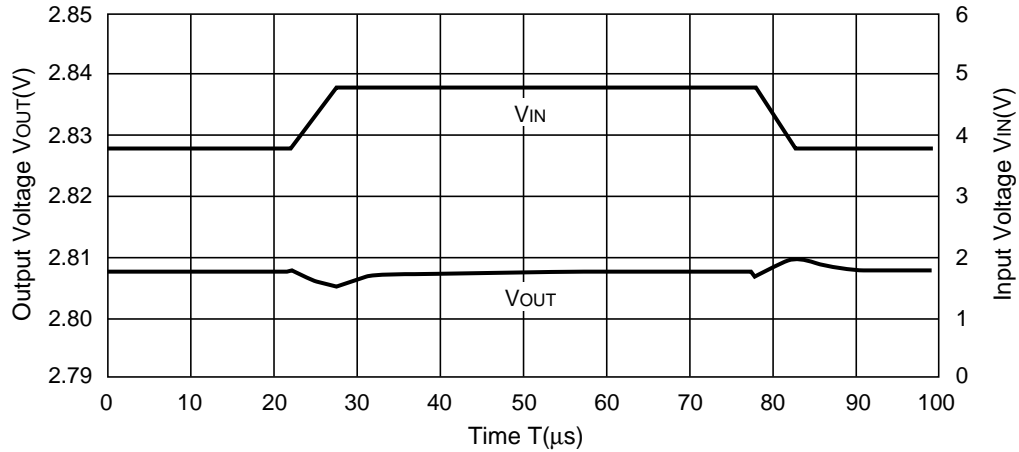
9) Ripple Rejection vs. Input Voltage (DC bias)  $C_{OUT} = \text{Ceramic } 1.0\mu\text{F}$  ( $T_{opt}=25^\circ\text{C}$ )



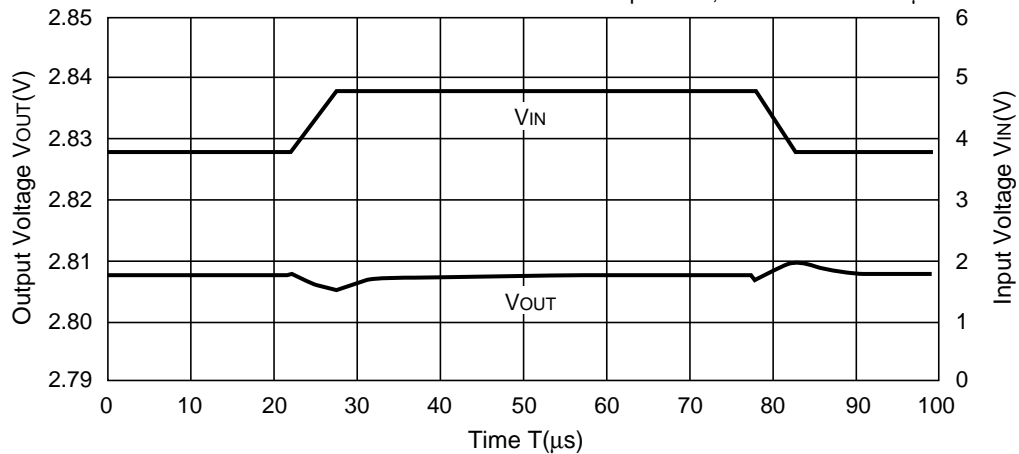


## 10) Input Transient Response

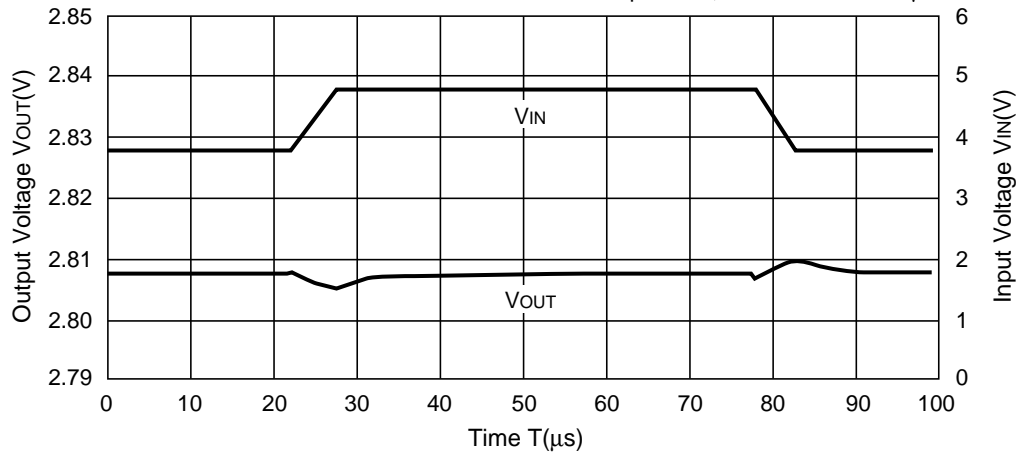
## R5323N001x(2.8V, VR1)

 $I_{OUT}=30\text{mA}$ ,  $t_r=t_f=5\mu\text{s}$ ,  $C_{OUT}=\text{Ceramic } 1.0\mu\text{F}$ 

## R5323N001x(2.8V, VR1)

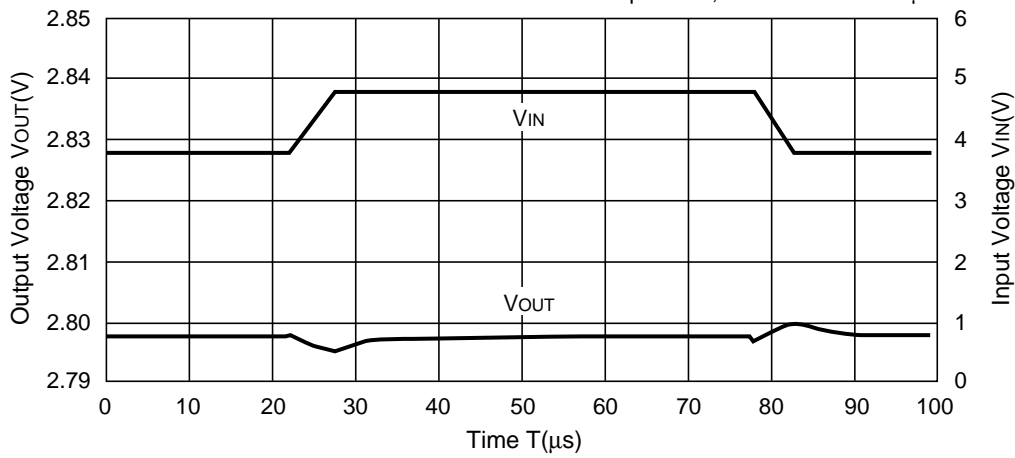
 $T_{opt}=25^\circ\text{C}$ ,  $C_{OUT}=\text{Ceramic } 2.2\mu\text{F}$ 

## R5323N001x(2.8V, VR1)

 $T_{opt}=25^\circ\text{C}$ ,  $C_{OUT}=\text{Ceramic } 4.4\mu\text{F}$ 

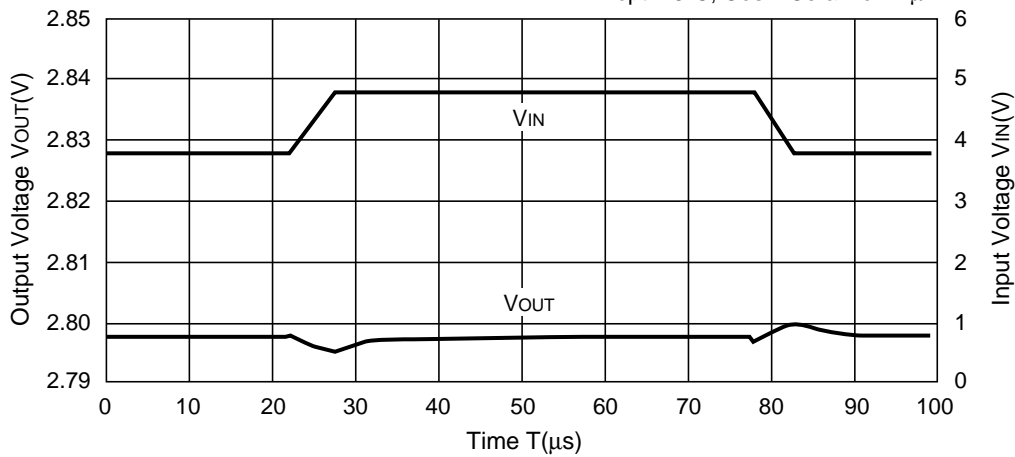
**R5323N001x(2.8V, VR2)**

Topt=25°C, COUT=Ceramic 1.0μF



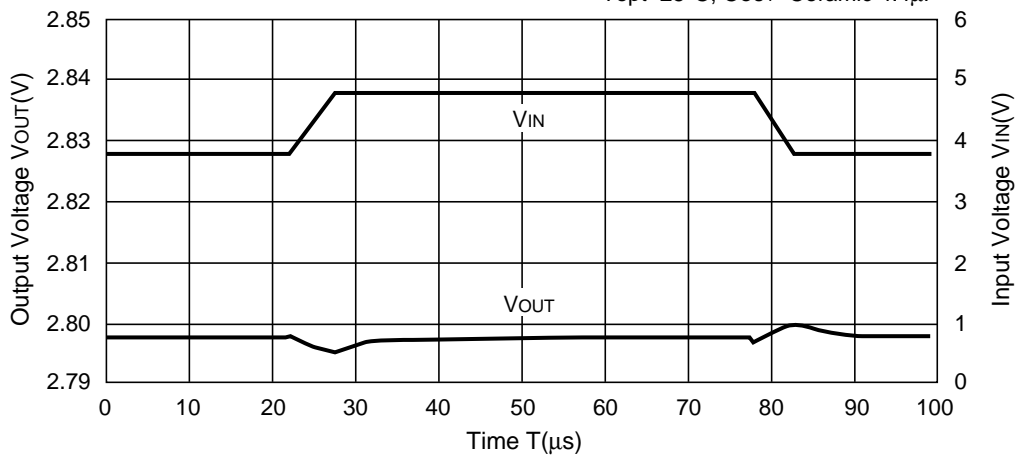
**R5323N001x(2.8V, VR2)**

Topt=25°C, COUT=Ceramic 2.2μF

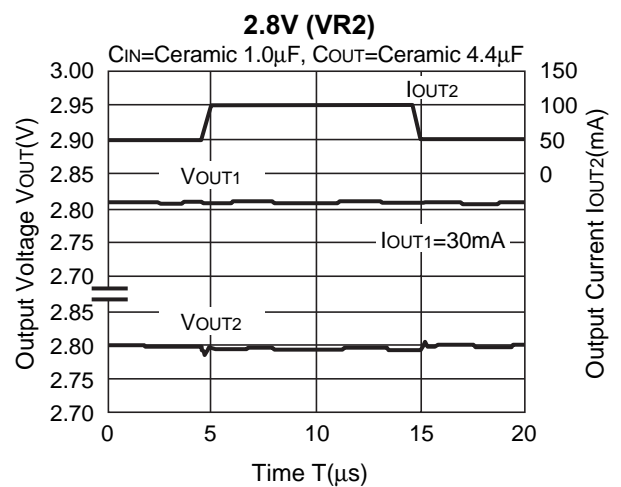
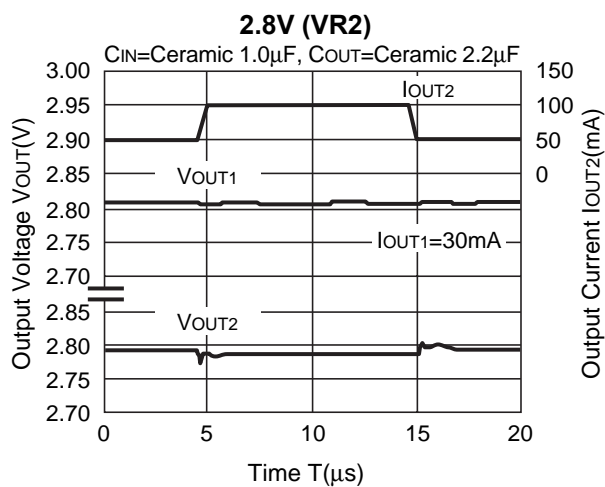
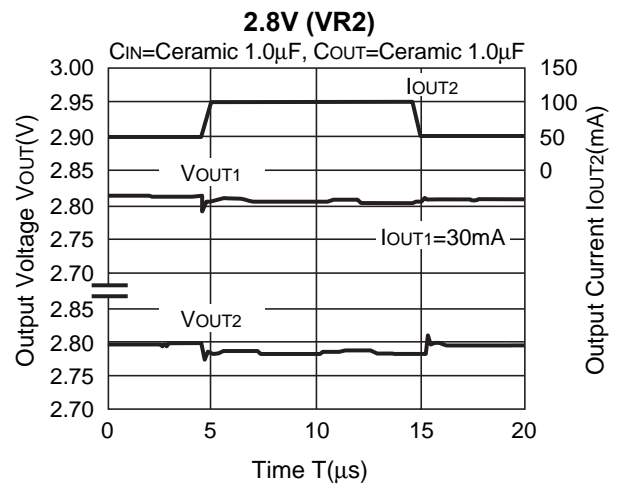
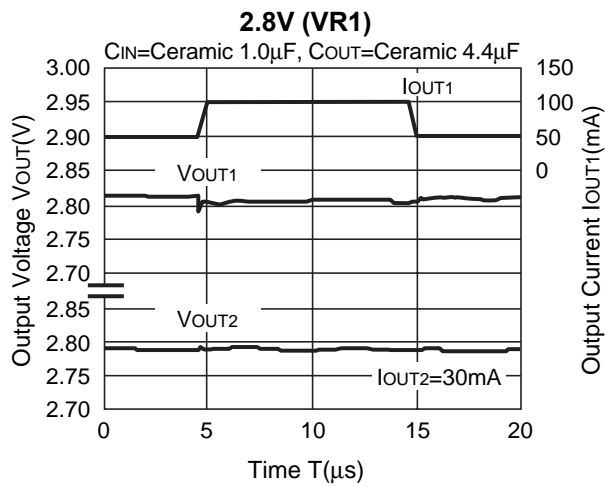
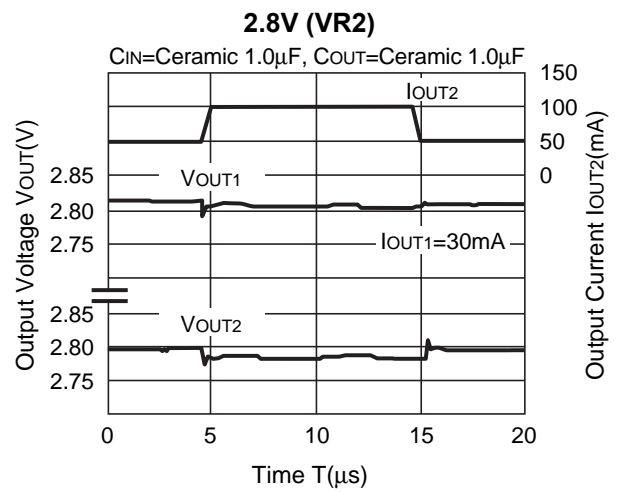
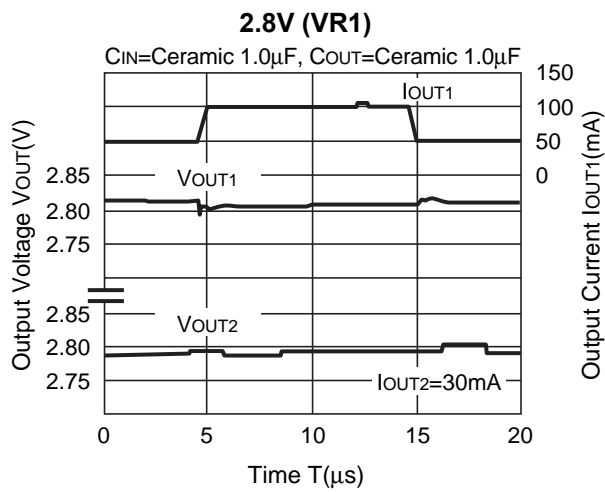


**R5323N001x(2.8V, VR2)**

Topt=25°C, COUT=Ceramic 4.4μF

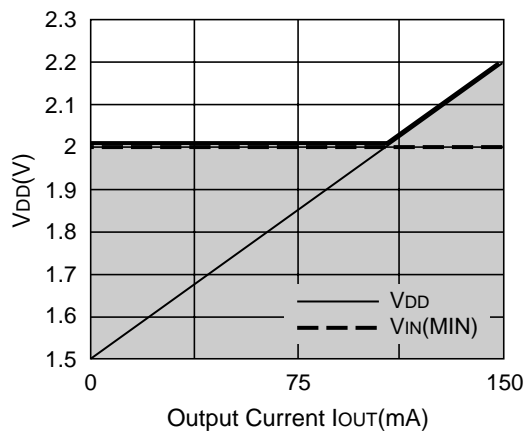


## 11) Load Transient Response



## 12) Minimum Operating Voltage

### 1.5V Minimum Operating Voltage Range



## TECHNICAL NOTES

When using these ICs, consider the following points:

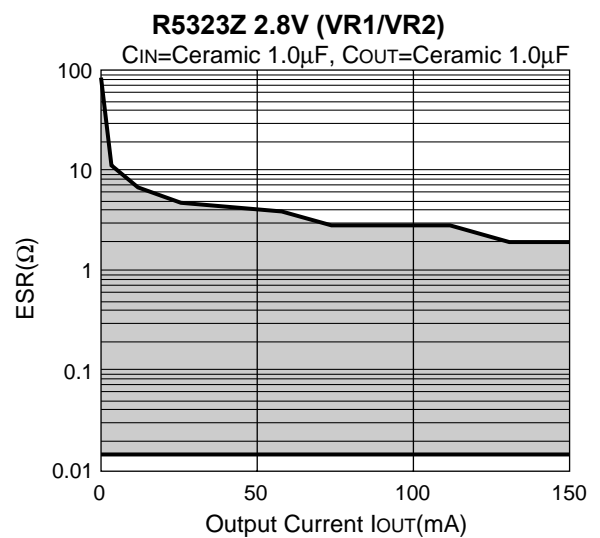
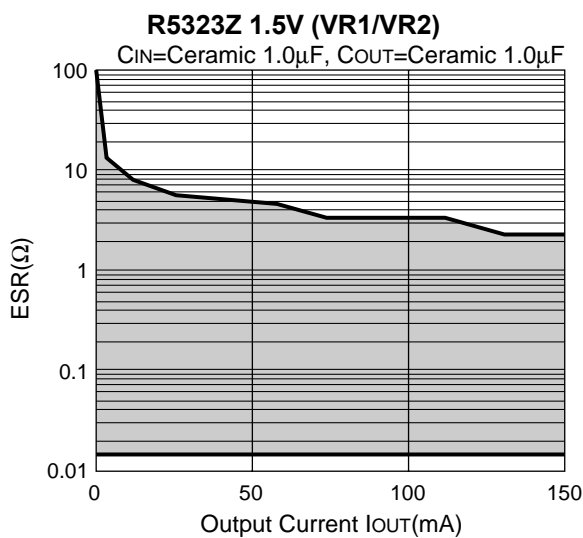
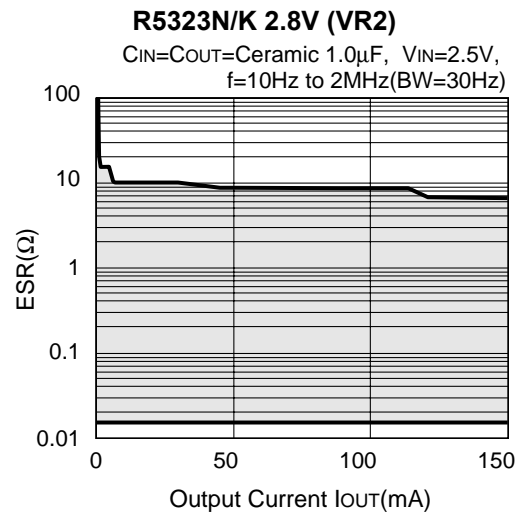
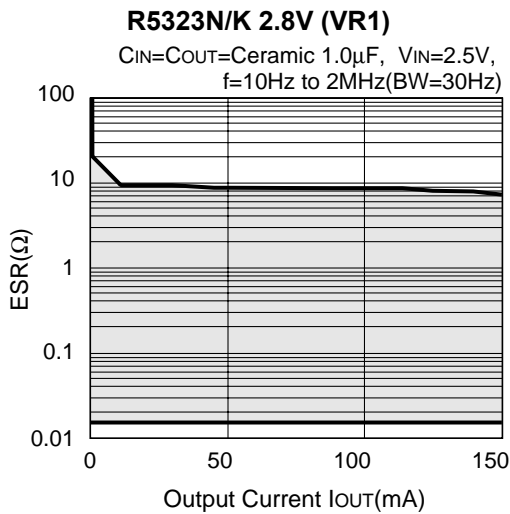
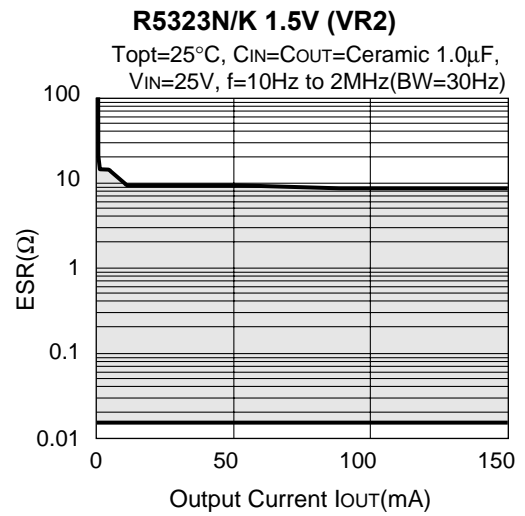
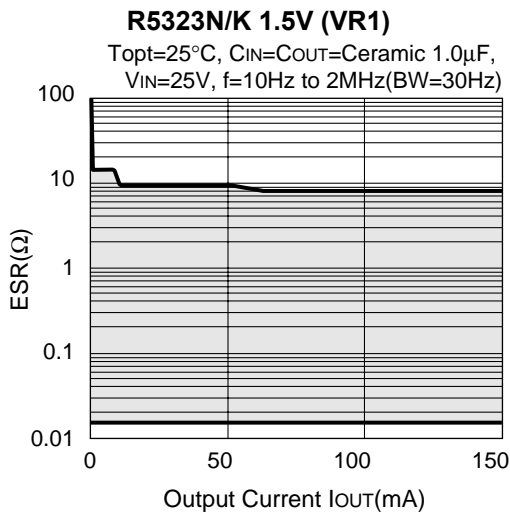
In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, be sure to use a  $1.0\mu\text{F}$  or more capacitance  $C_{OUT}$  with good frequency characteristics and ESR (Equivalent Series Resistance) of which is in the range described as follows:

The relations between  $I_{OUT}$  (Output Current) and ESR of Output Capacitor are shown in the typical characteristics above. The conditions when the white noise level is under  $40\mu\text{V}$  (Avg.) are marked as the hatched area in the graph.

Test these ICs with as same external components as ones to be used on the PCB.

- Make  $V_{DD}$  and GND lines sufficient. When their impedance is high, the noise pick-up or incorrect operation may result.
- Connect the capacitor with a capacitance of  $1\mu\text{F}$  or more between  $V_{DD}$  and GND as close as possible.
- Set external components, especially Output Capacitor, as close as possible to the ICs and make wiring as short as possible.

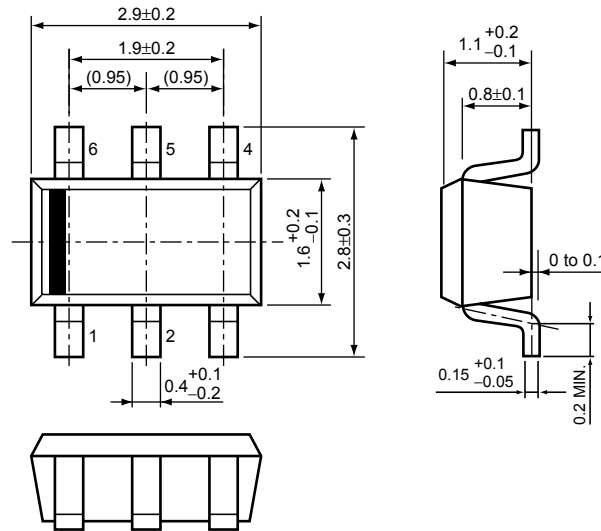
## ESR vs. Output Current



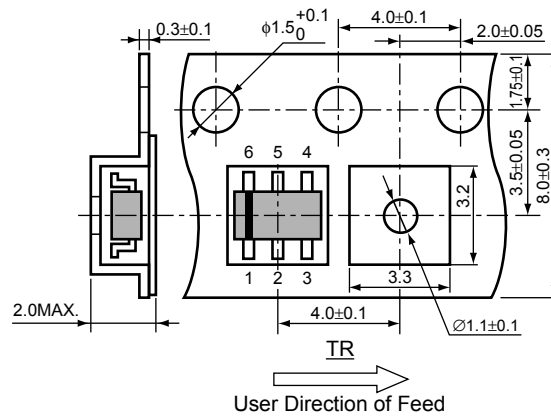
- SOT-23-6 (SC-74)

Unit: mm

**PACKAGE DIMENSIONS**

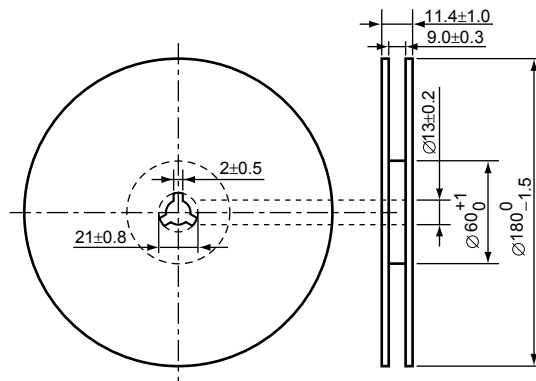


**TAPING SPECIFICATION**



**TAPING REEL DIMENSIONS**

(1reel=3000pcs)



### POWER DISSIPATION (SOT-23-6)

This specification is at mounted on board. Power Dissipation ( $P_D$ ) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

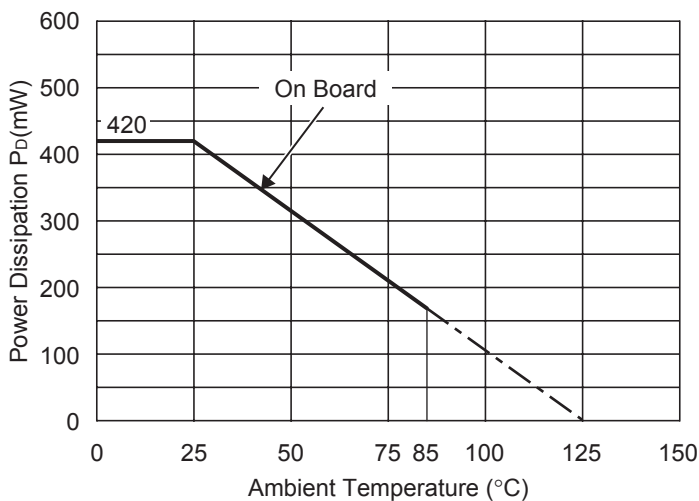
Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plactic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	φ0.5mm × 44pcs

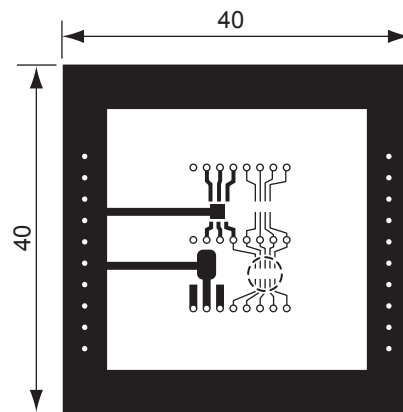
Measurement Result

( $T_{opt}=25^{\circ}C, T_{jmax}=125^{\circ}C$ )

	Standard Land Pattern	Free Air
Power Dissipation	420mW	250mW
Thermal Resistance	$\theta_{ja}=(125-25^{\circ}C)/0.42W=263^{\circ}C/W$	400°C/W



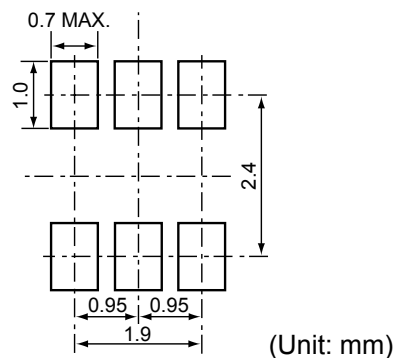
Power Dissipation



Measurement Board Pattern

○ IC Mount Area Unit : mm

### RECOMMENDED LAND PATTERN



(Unit: mm)





## POWER DISSIPATION (PLP1820-6)

This specification is at mounted on board. Power Dissipation ( $P_D$ ) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

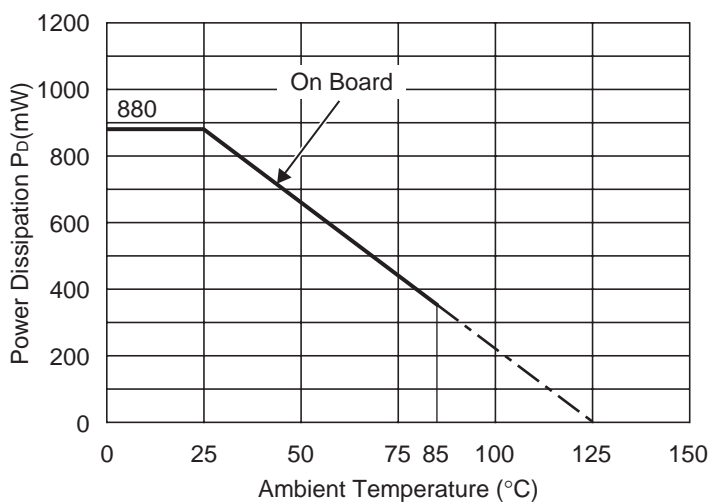
### Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plactic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	φ0.54mm × 30pcs

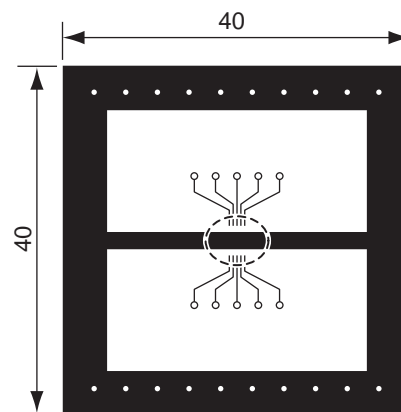
### Measurement Result

( $T_{opt}=25^{\circ}C, T_{jmax}=125^{\circ}C$ )

	Standard Land Pattern
Power Dissipation	880mW
Thermal Resistance	$\theta_{ja}=(125-25^{\circ}C)/0.88W=114^{\circ}C/W$



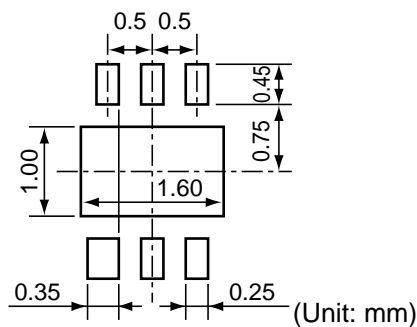
Power Dissipation



Measurement Board Pattern

○ IC Mount Area Unit : mm

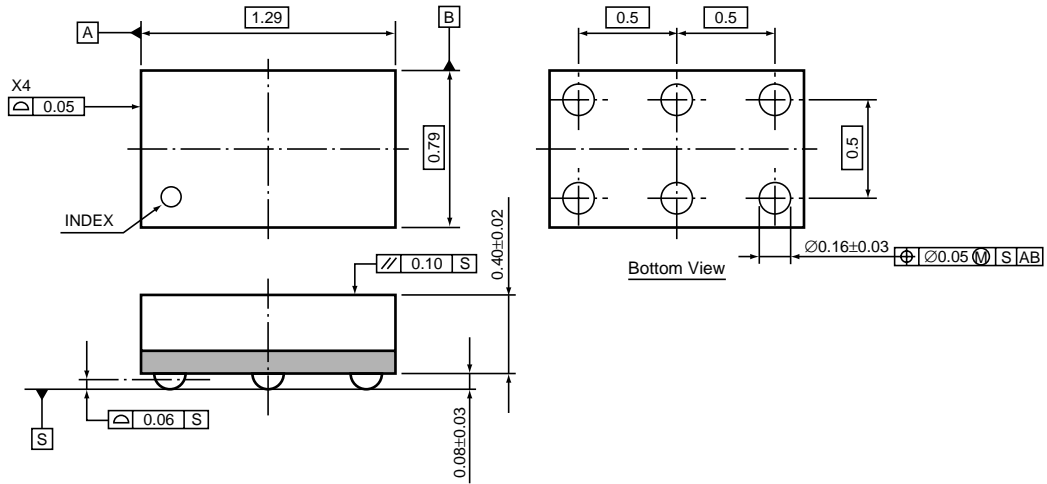
## RECOMMENDED LAND PATTERN



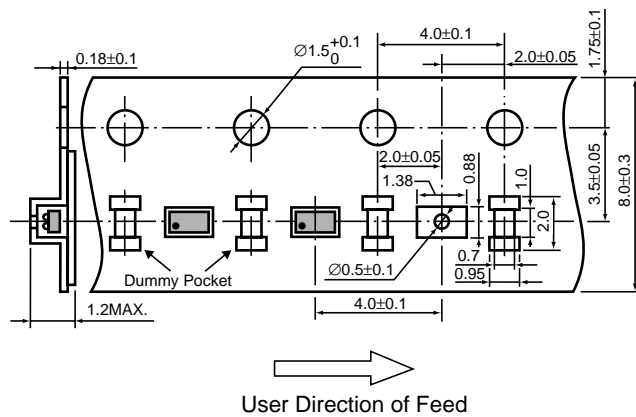
• WLCSP-6-P1

Unit: mm

PACKAGE DIMENSIONS



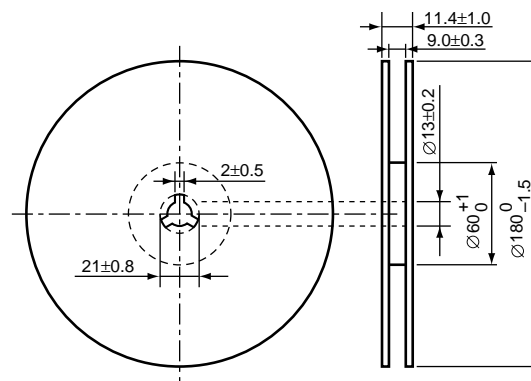
TAPING SPECIFICATION (TR: Standard Type)



➔ User Direction of Feed

TAPING REEL DIMENSIONS

(1reel=3000pcs)



## POWER DISSIPATION (WLCSP-6-P1)

This specification is at mounted on board. Power Dissipation ( $P_D$ ) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

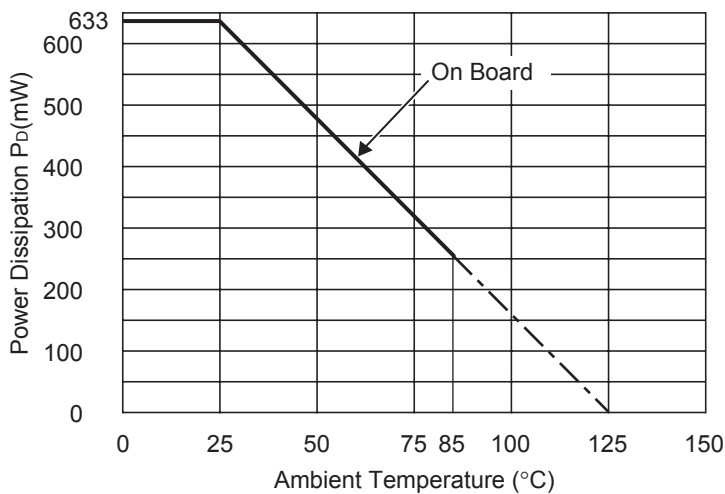
### Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plactic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	-

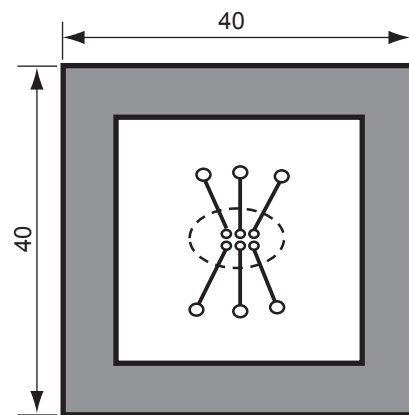
### Measurement Result

( $T_{opt}=25^{\circ}C, T_{jmax}=125^{\circ}C$ )

	Standard Land Pattern
Power Dissipation	633mW
Thermal Resistance	$\theta_{ja}=(125-25^{\circ}C)/0.633W=158^{\circ}C/W$



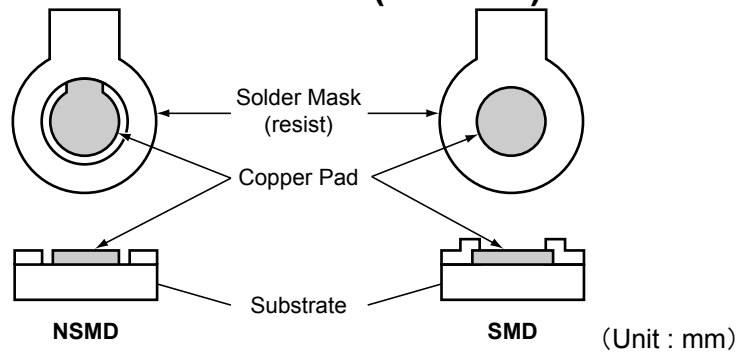
**Power Dissipation**



Measurement Board Pattern

○ IC Mount Area (Unit : mm)

**RECOMMENDED LAND PATTERN (WLCSP)**



**NSMD and SMD Pad Definition**

Pad definition	Copper Pad	Solder Mask Opening
NSMD (Non-Solder Mask defined)	0.20mm	Min. 0.30mm
SMD (Solder Mask defined)	Min. 0.30mm	0.20mm

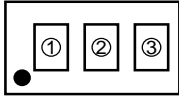
- \* Pad layout and size can be modified by customers material, equipment, method.
- \* Please adjust pad layout according to your conditions.
- \* Recommended Stencil Aperture Size.....ø0.3mm
- \* Since lead free WL-CSP components are not compatible with the tin/lead solder process, you shall not mount lead free WL-CSP components using the tin/lead solder paste.





## R5323Z SERIES MARK SPECIFICATION

### • WLCSP-6-P1



- ① : G (Fixed)
- ②, ③ : Lot Number

### • Product Code vs. Marking

Part Number	Product Code
	①
R5323Z001A	G
R5323Z002A	G
R5323Z003A	G
R5323Z004A	G
R5323Z005A	G
R5323Z006A	G
R5323Z007A	G
R5323Z008A	G
R5323Z009A	G
R5323Z010A	G
R5323Z011A	G
R5323Z012A	G
R5323Z013A	G
R5323Z014A	G
R5323Z015A	G
R5323Z016A	G
R5323Z017A	G
R5323Z018A	G
R5323Z019A	G
R5323Z020A	G

Part Number	Product Code
	①
R5323Z021A	G
R5323Z022A	G
R5323Z023A	G
R5323Z024A	G
R5323Z025A	G
R5323Z026A	G
R5323Z027A	G
R5323Z028A	G
R5323Z029A	G
R5323Z030A	G
R5323Z031A	G
R5323Z032A	G
R5323Z033A	G
R5323Z034A	G
R5323Z035A	G
R5323Z036A	G
R5323Z037A	G
R5323Z038A	G
R5323Z039A	G
R5323Z040A	G
R5323Z041A	G

Part Number	Product Code
	①
R5323Z001B	G
R5323Z002B	G
R5323Z003B	G
R5323Z004B	G
R5323Z005B	G
R5323Z006B	G
R5323Z007B	G
R5323Z008B	G
R5323Z009B	G
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R5323Z014B	G
R5323Z015B	G
R5323Z016B	G
R5323Z017B	G
R5323Z018B	G
R5323Z019B	G
R5323Z020B	G

Part Number	Product Code
	①
R5323Z021B	G
R5323Z022B	G
R5323Z023B	G
R5323Z024B	G
R5323Z025B	G
R5323Z026B	G
R5323Z027B	G
R5323Z028B	G
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R5323Z039B	G
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